output load detection circuit is utilizable in a driver circuit to control modulation current. Applicant refers the Examiner to FIGS. 3, 4 and 5 of the drawings, and the associated text at page 5, line 22 to page 9, line 28 of the specification. It is readily apparent from this portion of the application that the output load detection circuit 220 generates an output indicator, denoted FLAG, that is utilizable to control the modulation current IMOD. The specification at page 9, lines 7-13 describes this operation as follows:

> Referring again to FIG. 3, in the illustrative embodiment, the output indicator FLAG from circuit 220 is preferably supplied to a control logic circuit 225 which is associated with the laser driver 200 and is configured to shut down the IMOD current generation circuit when FLAG is at a logic high level. Upon connection of the proper load, the voltage at the OUTP and OUTN terminals will be pulled up above the load detection sense threshold. As a result, the output indicator FLAG will return to a logic low level, the IMOD current generation circuit will again be enabled, and the laser driver 200 returns to a normal operating mode.

It is to be appreciated that this is just one possible implementation of the claimed arrangement, and should not be construed as limiting the scope of the claims. Nonetheless, in view of the foregoing description, it is apparent that the limitation in question is not indefinite as alleged by the Examiner. The §112 rejection of claims 1, 15, 16 and 17 is thus believed to be improper, and should be withdrawn.

Claims 1, 5, 16 and 17 also stand rejected under §112, second paragraph, on the ground that use of the term "adapted to" in conjunction with the claimed current generator circuit is somehow improper. Applicant respectfully traverses the rejection. A current generator circuit adapted to establish a modulation current in the manner claimed is clearly and distinctly described in the specification, for example, at page 6, lines 4-7, which states that "[t]he current source I3 is arranged in a current generator circuit comprising transistors QA, QB and QC as shown" and that "[t]his current generator circuit generates the above-noted IMOD current." It is again to be appreciated that

numerous alternative implementations of the claimed arrangement may be used. It is respectfully submitted that Applicant is entitled to select claim language supported by the specification. In view of the foregoing example description from the specification, the term is question is believed to be proper and entitled to patentable weight. The §112 rejection based on usage of the term should therefore be withdrawn.

Claims 1, 2, 5 and 9-17 stand rejected under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,266,078 (hereinafter "Koga"). Applicant respectfully traverses the §102(a) rejection, for the reasons specified below.

Applicant initially notes that the Manual of Patent Examining Procedure (MPEP), Eight Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicant respectfully submits that the Examiner has failed to establish anticipation of at least independent claims 1, 16 and 17 by the Koga reference.

Each of independent claims 1, 16 and 17 calls for a driver circuit which includes an output load detection circuit having first and second inputs coupled to respective first and second outputs of an output stage of the driver circuit. The output load detection circuit is configured to detect an improper load condition at one or more of the first and second outputs of the output stage of the driver circuit and to generate a corresponding output indicator. The output indicator is utilizable in the driver circuit to control the modulation current so as to prevent saturation of at least one device in the output stage in the presence of the improper load condition.

Advantageously, the invention as claimed can prevent undesirable saturation of the output stage of a driver circuit under fault conditions, such as failure to connect a laser diode or other optical source to the driver circuit output prior to operation of the driver circuit, while also

maintaining the ability of the driver circuit to operate at high speeds. See the specification at, for example, page 1, line 26 to page 2, line 16 and page 3, lines 9-11.

Applicant submits that the Koga reference fails to teach or suggest at least the above-noted limitations of each of independent claims 1, 16 and 17, and furthermore fails to provide the associated advantages of the claimed invention.

The Examiner in formulating the §102(a) rejection argues that Koga in FIG. 5 thereof shows a driver circuit meeting the above-noted limitations of independent claims 1, 16 and 17. More specifically, the Examiner argues that the claimed output load detection circuit corresponds to the first and second comparators 145 and 146 of Koga. However, the comparators 145 and 146 of Koga are not configured as an output load detection circuit in the manner claimed. For example, comparators 145 and 146 do not collectively have first and second inputs coupled to respective first and second outputs of an output stage of a driver circuit. In addition, comparators 145 and 146 are not configured to detect an improper load condition at one or more of the first and second outputs of the output stage of the driver circuit. Moreover, any output indicator generated by the comparators 145 and 146 is not utilizable in the driver circuit to control the modulation current so as to prevent saturation of at least one device in the output stage of the driver circuit in the presence of the improper load condition.

Instead, the comparators 145 and 146 of Koga are part of a feedback control loop which simply detects and controls the optical output of lasers A and B of the multi-chip laser 110. A photodiode (PD) sensor 113 detects light emitted by the lasers A and B, and this signal is processed in a feedback loop comprising elements 141, 142, 143, 144 and 150, the comparators 145 and 146, and the logic circuit 147. The purpose of this laser optical output control arrangement, as described in column 8, lines 62-67 of Koga, is as follows:

> That is, by controlling the current of each bias current source so as to provide a target amount of light represented by the reference voltage VREF, APC control is performed in order to provide a desired amount of light of the corresponding semiconductor laser.

The Koga reference at column 1, lines 18-23 further describes conventional APC control techniques as follows:

> Conventionally, in a laser driving circuit of image forming apparatuses of this type, in order to protect a laser from being destructed, the output of the laser beam is monitored, and the driving current for the laser is limited or interrupted when the output exceeds a specified value.

The comparators 145 and 146 of Koga are thus used as part of a feedback control circuit for monitoring the optical output of the lasers A and B so as to protect the lasers. The present invention, by way of contrast, configures a driver circuit to include an output load detection circuit which can detect, among other improper load conditions, the failure to connect a laser diode or other optical source to the driver circuit prior to operating the driver circuit. The claimed arrangement advantageously protects the driver circuit itself under such conditions, by preventing the saturation of at least one device in the output stage thereof. As noted above, the Koga laser optical output control circuitry comprising comparators 145 and 146 is directed to an entirely different problem, and used for a different purpose. The comparators 145 and 146 and their associated circuitry thus fail to provide the previously-described advantages associated with the output load detection circuit in the claimed arrangements.

Accordingly, it is respectfully submitted that Koga fails to teach or suggest the limitations of each of independent claims 1, 16 and 17. The §102(a) rejection is believed to be improper and should be withdrawn.

Claims 3, 4 and 6-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Koga in view of U.S. Patent No. 5,883,910 (hereinafter "Link"). Applicant respectfully traverses the §103(a) rejection. The Link reference fails to supplement the above-described deficiencies of the Koga reference as applied to the corresponding independent claim 1. Claims 3, 4 and 6-8 are therefore believed allowable for at least the reasons identified above with regard to independent claim 1.

In view of the above, Applicant believes that claims 1-17 are in condition for allowance, and respectfully requests withdrawal of the §112, §102(a) and §103(a) rejections.

Respectfully submitted,

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